

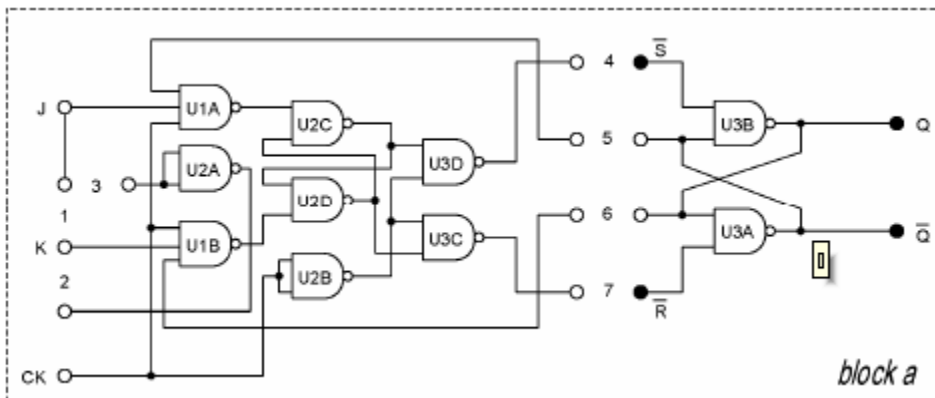
ID	Comp	Name

1. Objectives

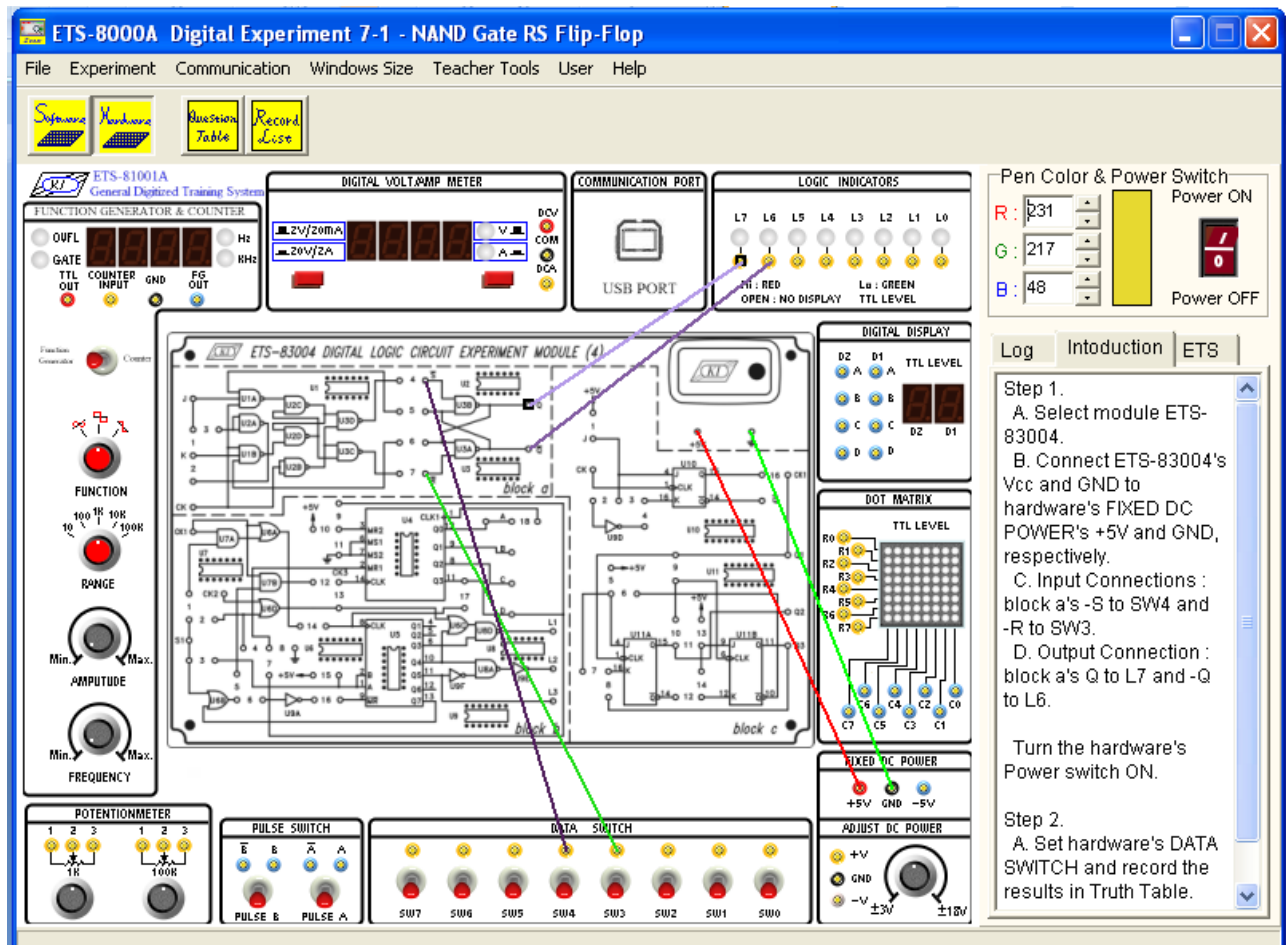
1. To study the operating principle of RS flip-flop.
2. To study the operating principle of JK flip-flop.
3. To study the operating principle of D and T flip-flop.

2. Experiment Steps

1. Place the ETS-83004 Module on the ETS-81001A Main unit.
2. Locate the block a on ETS-83004 Module as shown below.



3. Connect the input S' to DATA SWITCH SW4 and R' to SW3. Connect the outputs Q to Logic indicator L7 and Q' to L6.
4. Connect +5V and GND from FIXED DC POWER to ETS-83004 Module. Turn On the power.



5. Set Data Switches SW4 and SW3 as shown in the NAND gate RS flip-flop truth table below. Observe and record the L6 and L7 indications (red =1, green=0).

6. Results

Input		Output	
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
SW4	SW3	L7	L6
0	1		
1	1		
1	0		
1	1		
0	0		
1	0		
0	0		
0	1		

7. Remarks

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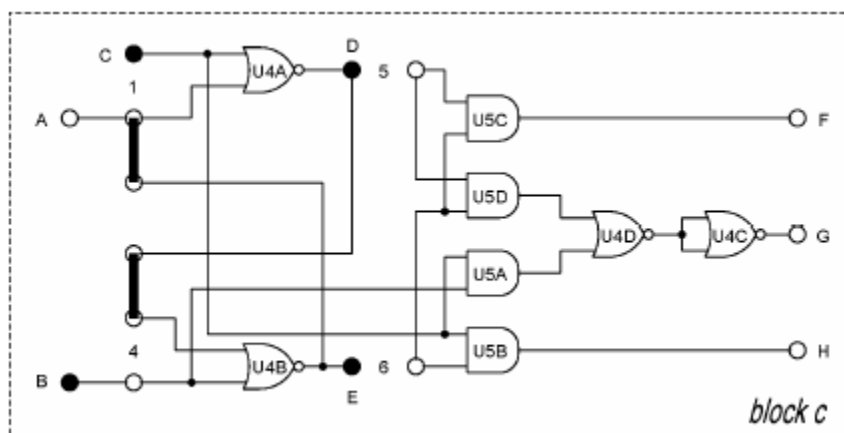
ID	Comp	Name

1. Objectives

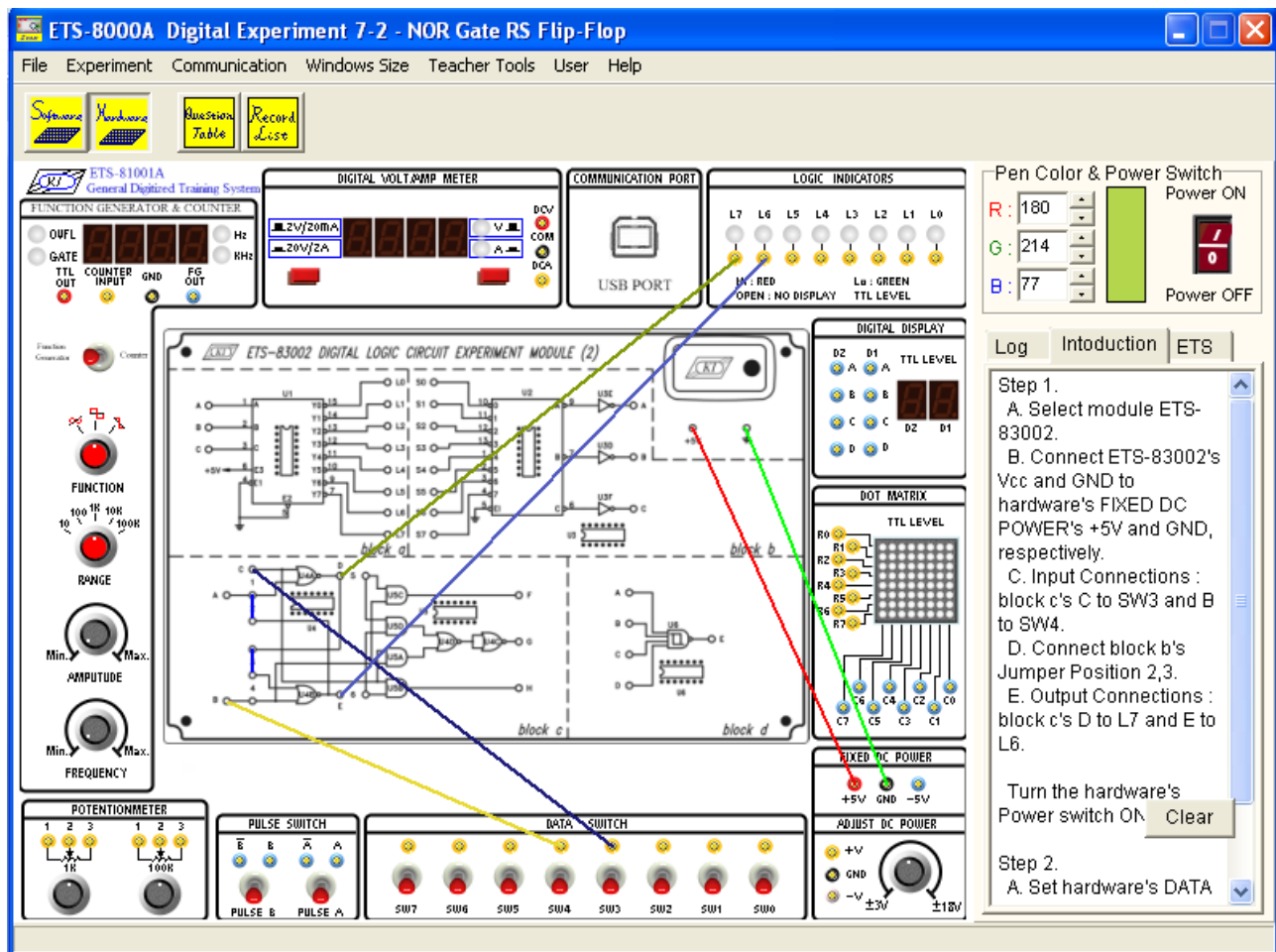
1. To study the operating principle of RS flip-flop.
2. To study the operating principle of JK flip-flop.
3. To study the operating principle of D and T flip-flop.

2. Experiment Steps

1. Place the ETS-83004 Module on the ETS-81001A Main unit.
2. Locate the block c on ETS-83002 Module as shown below.



3. Place jumpers in positions 2 and 3. Connect the input C to DATA SWITCH SW4 and B to SW3. Connect the outputs D to Logic indicator L7 and E to L6.
4. Connect +5V and GND from FIXED DC POWER to ETS-83002 Module. Turn On the power.



5. Set Data Switches SW4 and SW3 as shown in the NOR gate RS flip-flop truth table below. Observe and record the L6 and L7 indications (red =1, green=0).

6. Results

Input		Output	
S	R	Q	$\bar{Q}$
sw4	sw3	L7	L6
0	1		
0	0		
1	0		
0	0		
1	1		
1	0		
1	1		
0	1		

7. Remarks

[illegible]

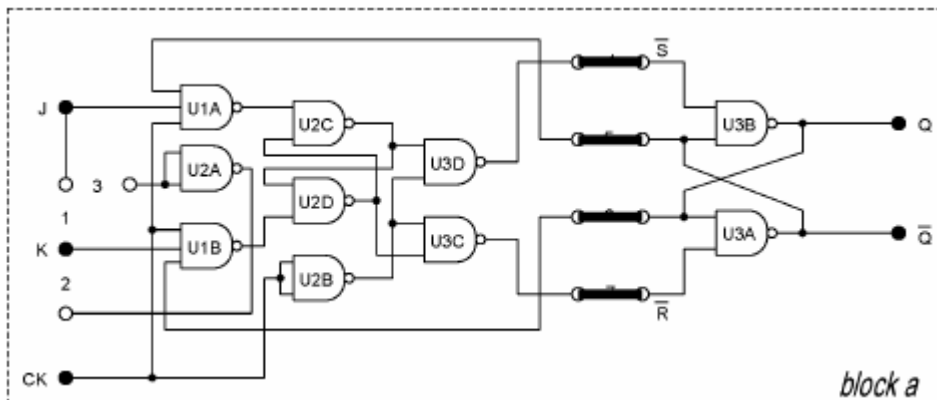
ID	Comp	Name

1. Objectives

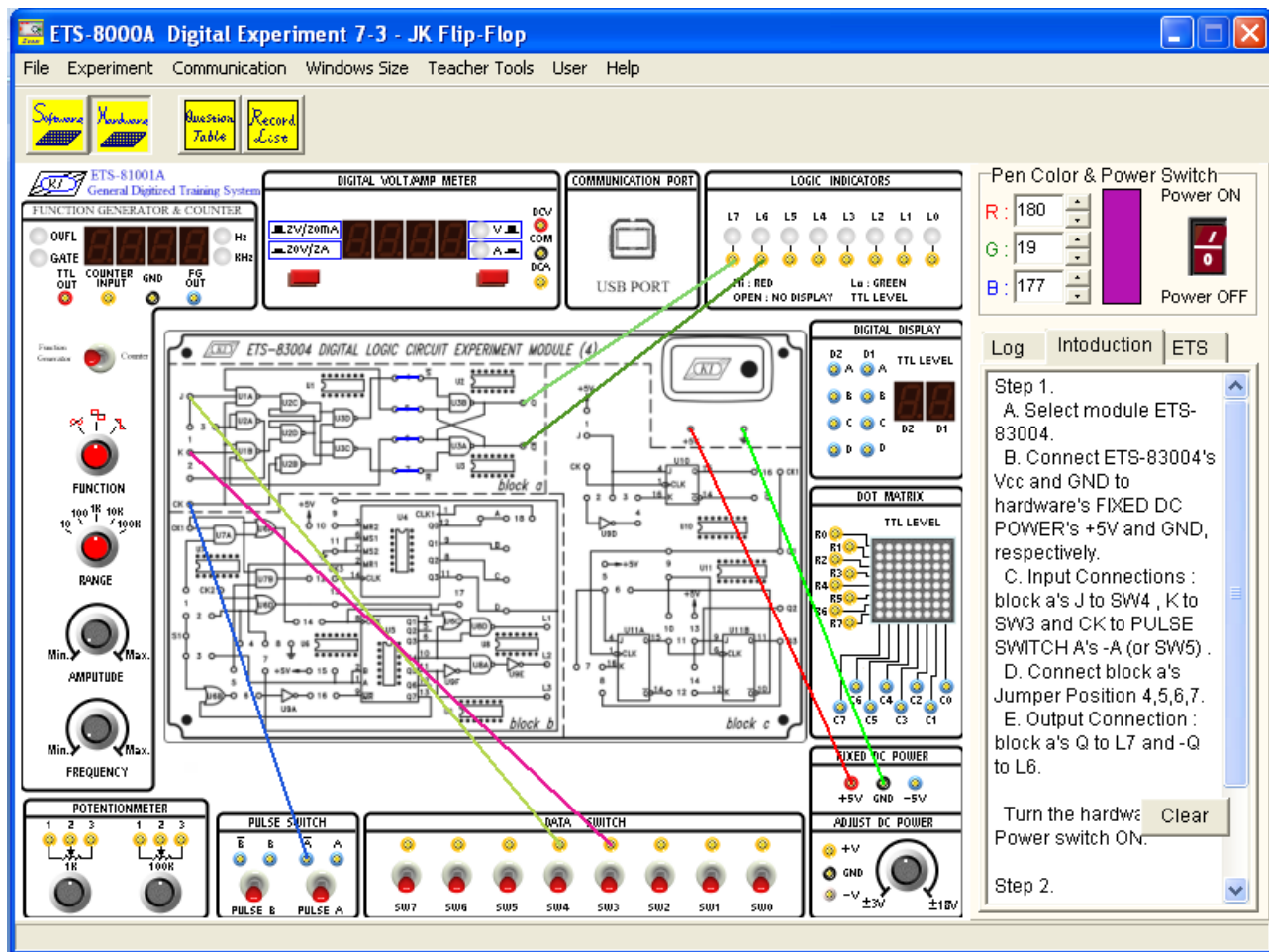
1. To study the operating principle of RS flip-flop.
2. To study the operating principle of JK flip-flop.
3. To study the operating principle of D and T flip-flop.

2. Experiment Steps

1. Place the ETS-83004 Module on the ETS-81001A Main unit.
2. Locate the block a on ETS-83004 Module as shown below.



3. Place jumpers in positions 4, 5, 6 and 7. Connect the input J to DATA SWITCH SW4 and K to SW3 and CK to SW5. Connect the outputs Q to Logic indicator L7 and Q' to L6.
4. Connect +5V and GND from FIXED DC POWER to ETS-83003 Module. Turn On the power.



5. Set Data Switches SW3- SW5 as shown in the master-slave JK flip-flop truth table below. Observe and record the L6 and L7 indications (red =1, green=0).

6. Results

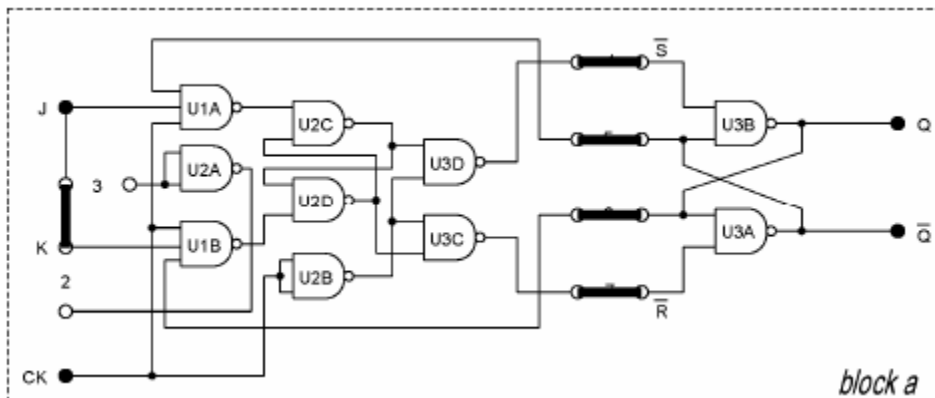
ID	Comp	Name

1. Objectives

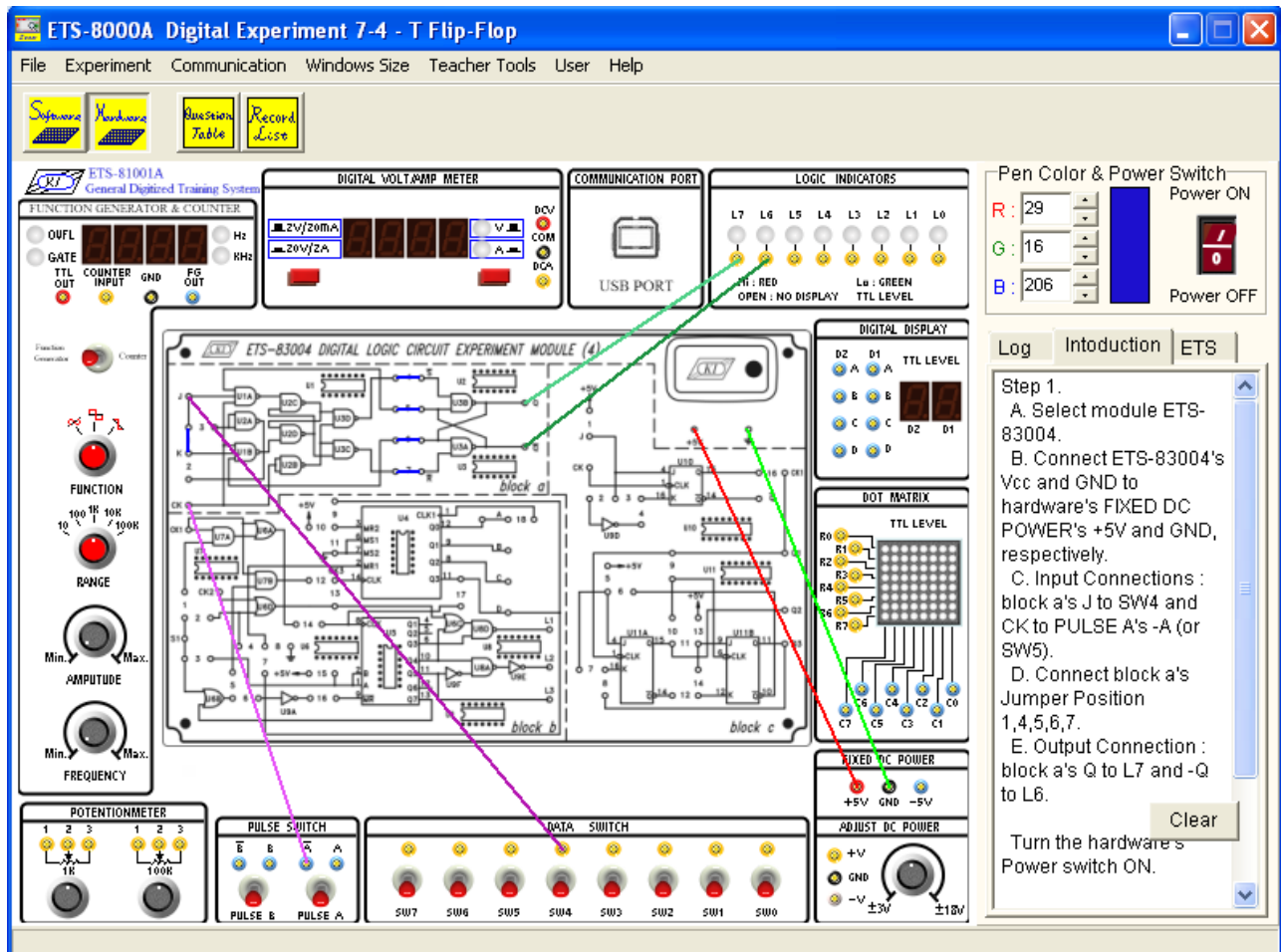
1. To study the operating principle of RS flip-flop.
2. To study the operating principle of JK flip-flop.
3. To study the operating principle of D and T flip-flop.

2. Experiment Steps

1. Place the ETS-83004 Module on the ETS-81001A Main unit.
2. Locate the block a on ETS-83004 Module as shown below.



3. Place jumpers in positions 1, 4, 5, 6 and 7. Connect the input J to DATA SWITCH SW4 and CK to SW5. Connect the outputs Q to Logic indicator L7 and Q' to L6.
4. Connect +5V and GND from FIXED DC POWER to ETS-83003 Module. Turn On the power.



5. Set Data Switches SW4 and SW5 as shown in the master-slave T flip-flop truth table below. Observe and record the L6 and L7 indications (red =1, green=0).

6. Results

Input		Output	
CK	T	Q	$\bar{Q}$
SW5	SW4	L7	L6
	0		
	0		
	1		
	1		

Note :  stands for 0 → 1 → 0.

7. Remarks

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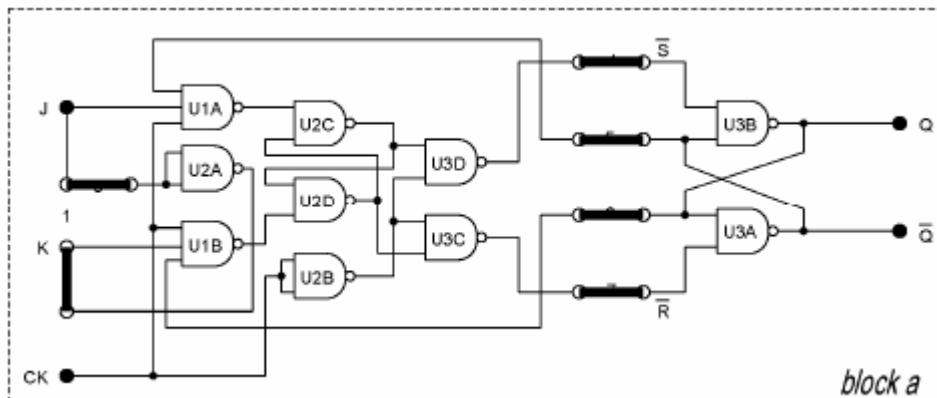
ID	Comp	Name

1. Objectives

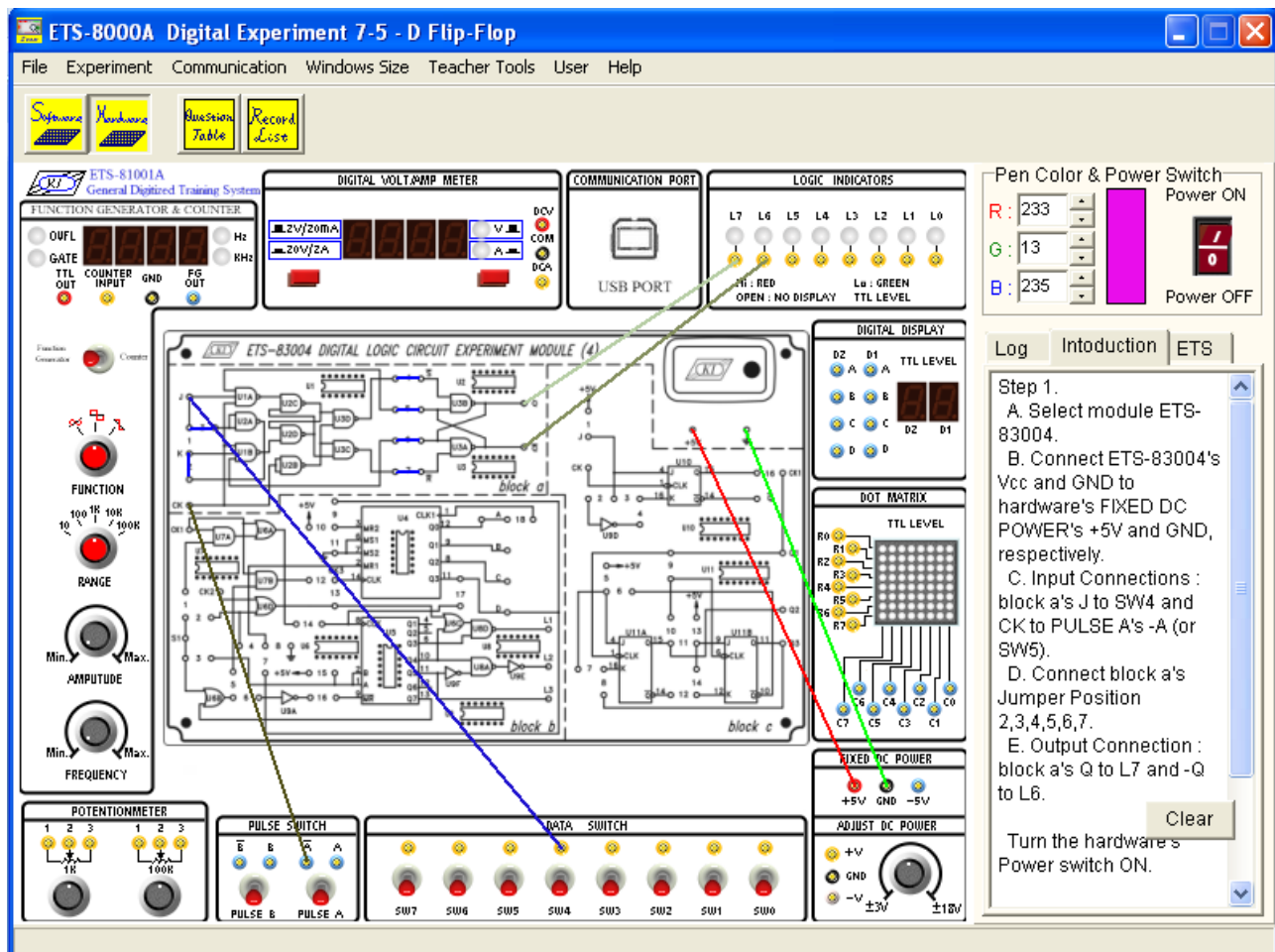
1. To study the operating principle of RS flip-flop.
2. To study the operating principle of JK flip-flop.
3. To study the operating principle of D and T flip-flop.

2. Experiment Steps

1. Place the ETS-83004 Module on the ETS-81001A Main unit.
2. Locate the block a on ETS-83004 Module as shown below.



3. Place jumpers in positions 1, 4, 5, 6 and 7. Connect the input J to DATA SWITCH SW4 and CK to SW5. Connect the outputs Q to Logic indicator L7 and Q' to L6.
4. Connect +5V and GND from FIXED DC POWER to ETS-83003 Module. Turn On the power.



- Set Data Switches SW4 and SW5 as shown in the master-slave T flip-flop truth table below. Observe and record the L6 and L7 indications (red =1, green=0).

6. Results

Input		Output	
CK	D	Q	$\bar{Q}$
SW5	SW4	L7	L6
	0		
	1		
	0		
	1		

Note :  stands for $0 \rightarrow 1 \rightarrow 0$.

7. Remarks

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